IN THE CLAIMS

Please amend the claims to read as indicated herein.

1. (original) A circuit comprising:

a decoder for receiving an address within an address space of a processor and for accessing a pixel in an active pixel sensor array based on said address,

wherein said decoder maps said active pixel sensor array to said address space.

2. (original) The circuit of claim 1, wherein said decoder converts said address into a row signal and a column signal that designate a position of said pixel in said active pixel sensor array.

3. (original) The circuit of claim 1, further comprising:

a module for receiving a start address and an end address that designates a portion of said active pixel sensor array,

wherein said module uses said start address and said end address to present a sequence of addresses that said decoder uses to sequentially access a plurality of pixels in said portion.

4. (original) The circuit of claim 1, further comprising a module for correcting for a condition selected from the group consisting of: an offset of said pixel, and a gain of said pixel.

5. (original) The circuit of claim 1,

wherein said active pixel sensor array senses an image, and

wherein said circuit is employed for tracking a target in said image.

6. (original) The circuit of claim 5, wherein said target is a star.

7. (original) The circuit of claim 1,

wherein said pixel is one of a plurality of pixels in said active pixel sensor array, and

wherein said circuit provides a signal to simultaneously extract charges from said plurality of pixels.

8. (original) The circuit of claim 7, wherein said plurality of pixels form a row of pixels in said active pixel sensor array.

9. (original) The circuit of claim 7, wherein said charges are added together to yield a sum.

10. (original) The circuit of claim 9, further comprising a module for comparing said sum to a threshold value to determine whether a target image is represented by said plurality of pixels.

11. (original) An integrated circuit, comprising:
an active pixel sensor array, and
a decoder for receiving an address within an address space of a processor and for accessing a pixel of said active pixel sensor array based on said address,
wherein said decoder maps said active pixel sensor array to said address space.

12. (original) The integrated circuit of claim 11, further comprising a converter for representing a charge read from said pixel as a digital value.

13. (original) The integrated circuit of claim 11, wherein said active pixel sensor array is configured of complementary metal oxide semiconductor (CMOS) devices.

14. (original) The integrated circuit of claim 11, wherein said decoder accesses said pixel by converting said address into a row signal and a column signal to designate a position of said pixel in said active pixel sensor array.

15. (original) The integrated circuit of claim 11, further comprising an module for receiving a start address and an end address that designates a portion of said active pixel sensor array, wherein said module uses said start address and said end address to present a sequence of addresses to said decoder to access pixels in said portion.

16. (original) The integrated circuit of claim 11, further comprising a module to correct for a condition selected from the group consisting of: an offset of said pixel, and a gain of said pixel.

17. (original) The integrated circuit of claim 11, further comprising an amplifier for amplifying a charge read from said pixel.

18. (original) The integrated circuit of claim 11, wherein said pixel comprises an electron well and a gate to control integration time over said electron well.

19. (original) The integrated circuit of claim 11, wherein said pixel comprises a photodiode to collect a charge.

20. (original) The integrated circuit of claim 11, wherein said active pixel sensor array senses an image, and wherein said integrated circuit is employed for tracking a target in said image.

21. (original) The integrated circuit of claim 20, wherein said target is a star.

22. (original) An interface comprising a module that enables a processor to access a pixel circuit in an active pixel sensor array by direct memory access.

23. (currently amended) The interface of claim 22,

wherein said module comprises a decoder for receiving an address from said processor, and for converting said address into a row signal and a column signal that designate a position of said pixel circuit in said active pixel sensor array,

wherein said address is within an address space of said processor, and

wherein said decoder maps said active pixel sensor array to said address space.

24. (original) The interface of claim 22, further comprising a module for receiving a start address and an end address and for sequentially accessing a plurality of pixel circuits in a portion of said active pixel sensor array based on said start address and said end address.

25. (original) The interface of claim 22, further comprising a module for correcting for a condition selected from the group consisting of: an offset of said pixel circuit, and a gain of said pixel circuit.

26. (original) The interface of claim 22,
wherein said active pixel sensor array senses an image, and
wherein said interface is employed for tracking a target in said image.

27. (original) The interface of claim 26, wherein said target is a star.

28. (original) The interface of claim 22,
wherein said pixel circuit is one of a plurality of pixel circuits in said active pixel sensor array, and
wherein said interface provides a signal to simultaneously extract charges from said plurality of pixel circuits.

29. (original) The interface of claim 28, wherein said plurality of pixel circuits form a row of pixel circuits in said active pixel sensor array.

30. (original) The interface of claim 28, wherein said charges are added together to yield a sum.

31. (original) The interface of claim 30, further comprising a module for comparing said sum to a threshold value to determine whether a target image is represented by said plurality of pixel circuits.

32. (original) A system comprising:

an active pixel sensor array;

a decoder for accessing a pixel of said active pixel sensor array based on an address;

a converter for representing a charge read from said pixel as a digital value; and

a microprocessor for providing said address and receiving said digital value,

wherein said address is within an address space of said microprocessor, and

wherein said decoder maps said active pixel sensor array to said address space.

33. (original) The system of claim 32, wherein said active pixel sensor array is configured of complementary metal oxide semiconductor (CMOS) devices.

34. (original) The system of claim 32, wherein said decoder accesses said pixel by converting said address into a row signal and a column signal to designate a position of said pixel in said active pixel sensor array.

35. (original) The system of claim 32,

wherein said microprocessor provides a start address and an end address that designates a portion of said active pixel sensor array, and

wherein said system further comprises a module that uses said start address and said end address to present a sequence of addresses to said decoder to access pixels in said portion.

36. (original) The system of claim 32, further comprising a module to correct for a condition selected from the group consisting of: an offset of said pixel, and a gain of said pixel.

37. (original) The system of claim 32, further comprising an amplifier for amplifying a charge read from said pixel.

38. (original) The system of claim 32, wherein said active pixel sensor array senses an image, and said system is employed for tracking a target in said image.

39. (original) The system of claim 38, wherein said target is a star.

40. (original) The system of claim 32, wherein said pixel wherein said microprocessor controls an integration time for a window that includes said pixel.

41. (original) The system of claim 32, wherein said microprocessor controls an integration time on a group of pixels of said active pixel sensor array.

42. (original) The system of claim 32, wherein said microprocessor addresses a sub-frame of view region of said active pixel sensor array.

43. (original) The system of claim 32, wherein said microprocessor manages a first sub-frame of said active pixel sensor array and a second sub-frame of said active pixel sensor array.

44. (original) The system of claim 43, wherein said first sub-frame has a first integration time and said second sub-frame has a second integration time.

45. (original) The system of claim 43, wherein said first and second sub-frame of view regions overlap one another.